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L3: Entry 1 of 1 File: JPAB Apr 9, 1993

PUB-NO: JP405090262A
DOCUMENT-IDENTIFIER: JP 05090262 A
TITLE: SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUBN-DATE: April 9, 1993

INVENTOR-INFORMATION:

NAME	COUNTRY
MIZUSHIMA, KAZUYUKI	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	

APPL-NO: JP03248668
APPL-DATE: September 27, 1991

US-CL-CURRENT: 438/678; 438/FOR.390
INT-CL (IPC): H01L 21/3205; H01L 21/302; H01L 21/318

ABSTRACT:

PURPOSE: To realize a fine multilayer interconnection excellent in accuracy independent of a lower wiring high or low in density.

CONSTITUTION: A first insulating film 7 thicker than a wiring film is previously formed on a semiconductor substrate 1 where an element has been formed, and a first conductive film 8 is foamed thereon to serve as the electricity feed layer for electroplating A recessed groove 10 is formed on a wiring forming region, and a second conductive film 11 is formed to be enhanced in adhesion to an insulating film and to feed an electric power. Then, a side wall 13 of insulating film is formed on the side wall of the groove. In succession, a plated conductor 14 is formed inside the groove through electroplating to serve as a wiring. By this setup, as the surface of the insulating film is level with that of a wiring, a fully flat multilayer interconnection can be realized.

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L1: Entry 5 of 8 File: JPAB Oct 31, 1997

PUB-NO: JP409283520A
DOCUMENT-IDENTIFIER: JP 09283520 A
TITLE: MULTI-STEP BURIED WIRING STRUCTURE OF INTEGRATED CIRCUIT AND MANUFACTURE THEREOF

PUBN-DATE: October 31, 1997

INVENTOR-INFORMATION:
NAME COUNTRY
MORI, TAKESHI
TOYODA, YOSHIHIKO
FUKADA, TETSUO
HASEGAWA, MAKIKO

ASSIGNEE-INFORMATION:
NAME COUNTRY
MITSUBISHI ELECTRIC CORP

APPL-NO: JP08089507
APPL-DATE: April 11, 1996

INT-CL (IPC): H01 L 21/3205; H01 L 23/522

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent the halation of exposure light from being generated on the surface of a conductive layer by a method wherein a conductive coating layer having a function to prevent the exposure light from reflecting at the time of patterning a second insulating layer is formed on the conductive layer.

SOLUTION: A first buried groove for wiring use is formed in a first insulating layer 2 on a semiconductor substrate 1. A first conductive layer 4 and a conductive coating layer 6, which has a continuity with the layer 4 and has a function to prevent exposure light from reflecting at the time of a patterning of a second insulating layer 7, are buried in the groove 12 in order. The layer 7 is formed on the layer 2 and the layer 6 and a via hole 8 is formed on the layer 6 in the layer 7. A conductive connection part 9, which makes a continuity with the layer 6, is buried in the via hole 8. A second conductive layer 14 is buried in a second buried groove in a third insulating layer 10. Thereby, it becomes possible to form the via hole and the conductive connection part buried in the via hole with high accuracy.

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L1: Entry 1 of 8 File: JPAB Nov 24, 2000

PUB-NO: JP02000323479A
DOCUMENT-IDENTIFIER: JP 2000323479 A
TITLE: SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUBN-DATE: November 24, 2000

INVENTOR-INFORMATION:
NAME COUNTRY
HASEGAWA, TOSHIAKI
TAGUCHI, MITSURU
MIYATA, KOJI
IKEDA, KOICHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
SONY CORP

APPL-NO: JP11133533
APPL-DATE: May 14, 1999

INT-CL (IPC): H01 L 21/3205; H01 L 21/768

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent migration of copper in a copper wiring from an interface between a barrier metal layer and a nitride layer to an interlayer insulating film and thus to prevent the occurrence of a leak current and a short circuit between neighboring wirings, by simply covering the upper surface of the copper wiring formed in a wiring trench via a barrier metal layer with a nitride film.

SOLUTION: A semiconductor device having a wiring 24 formed in a recessed portion (wiring trench) 22 formed in an interlayer insulating film 21 has a first barrier layer 23 covering the wiring 24 from under the wiring 24, and a second barrier layer 25 covering the wiring 24 from over the wiring 24, wherein the first barrier layer 23 overlaps the second barrier layer 25.

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L1: Entry 3 of 8 File: JPAB Aug 31, 1999

PUB-NO: JP411238712A
DOCUMENT-IDENTIFIER: JP 11238712 A
TITLE: METHOD AND APPARATUS FOR CHEMICAL MECHANICAL POLISHING

PUBN-DATE: August 31, 1999

INVENTOR-INFORMATION:
NAME COUNTRY
NAKADA, KENSUKE
KIMURA, TAKESHI
NEZU, HIROKI
KOJIMA, HIROYUKI
HIRAI, OSAMU
ITO, HIDEFUMI

ASSIGNEE-INFORMATION:
NAME COUNTRY
HITACHI LTD

APPL-NO: JP10057477
APPL-DATE: February 23, 1998

INT-CL (IPC): H01 L 21/304; H01 L 21/304; B24 B 37/04; H01 L 21/3205

ABSTRACT:

PROBLEM TO BE SOLVED: To determine a termination point automatically and positively.

SOLUTION: A pair of electrodes 41 are put at a head 31 of a chemical mechanical polishing machine. An ohmmeter 42 for measuring parallel electric resistance is provided across the electrodes 41. In chemical mechanical polishing, the parallel electric resistance of a metal film 10 and a polishing solution 26 is measured by the ohmmeter 42. When a damascene wiring is formed after the polishing, the parallel electric resistance increases to a large value, so an increasing point is determined as a termination point using a termination point determining device 43. In this way the termination point of chemical mechanical polishing for forming the damascene wiring is determined automatically, and a defective state due to excess or shortage of polishing can be prevented.

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L1: Entry 7 of 8 File: JPAB May 31, 1996

PUB-NO: JP408139060A
DOCUMENT-IDENTIFIER: JP 08139060 A
TITLE: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE AND CHEMICAL MACHINE POLISHER

PUBN-DATE: May 31, 1996

INVENTOR-INFORMATION:
NAME COUNTRY
FUSE, AKIHIRO

ASSIGNEE-INFORMATION:
NAME COUNTRY
RICOH CO LTD

APPL-NO: JP06295582
APPL-DATE: November 4, 1994

INT-CL (IPC): H01 L 21/304; H01 L 21/3205

ABSTRACT:

PURPOSE: To bury a metal in a connecting hole for flattening the surface of an insulating film using a chemomechanical polishing step comprising a series of processes.

CONSTITUTION: An interlayer insulating film 3 is formed on a metallic wiring 2 formed on a semiconductor substrate 1 and after the formation of a connecting hole in the interlayer insulating film 3, a metallic film 6 is formed on the interlayer insulating film 3. This metallic film 6 is polished using an acid polishing solution in a chemomechanical polishing process. In this chemomechanical polishing process, the surface exposed time point of the surface of the interlayer insulating film 3 to the polished surface is detected by the change of revolving torque of a carrier head or the conductivity in the wafer thickness direction to continue the polishing of the metallic film as it is assuming the detection time as the terminal time. Later, the feeding of the polishing solution is stopped to be substituted for pure water for linsing step and then substituting for alkalic polishing solution for insulating film for polishing the interlayer insulating film 3 for flattening the surface. In the polishing step, the metal 6 buried in the connecting hole 4 is used as the polishing stopper of the interlayer insulating film 3.

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L1: Entry 2 of 8 File: JPAB Nov 30, 1999

PUB-NO: JP411330246A
DOCUMENT-IDENTIFIER: JP 11330246 A
TITLE: MUTUAL INTERCONNECTION OF COPPER AND ITS MANUFACTURE

PUBN-DATE: November 30, 1999

INVENTOR-INFORMATION:
NAME COUNTRY
RABIURU, ISURAM
ABGELINOS, V GERATOS
KEVIN, LUCAS
FILIPIAK, STANLEY M
RAMUNAS, BENKATORAMAN

ASSIGNEE-INFORMATION:
NAME COUNTRY
MOTOROLA INC

APPL-NO: JP11097400
APPL-DATE: April 5, 1999

INT-CL (IPC): H01 L 21/768; H01 L 21/3205

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a mutual interconnection of copper and a method of manufacturing which are capable of reliability enhancement in a semiconductor device, by exposing a mutual copper interconnection member to hydrogen- containing plasma, forming copper oxide from outside, and inhibiting oxidization a clarified copper layer again before forming a copper barrier layer on the surface.

SOLUTION: A mutual copper interconnection member 39 is formed in an opening for mutual interconnection after removing a second copper layer, a first copper layer and a conductive barrier layer. A copper barrier layer 40 consisting of silicon and nitrogen is formed on the mutual copper interconnection member 39. The mutual copper interconnection member 39 is exposed to hydrogen-containing silicon-free plasma. Copper oxide is removed from an exposed part of the mutual copper interconnection member 39. The processed substrate is cleaned in the same chamber as that of the copper barrier layer, so that the cleaned copper surface is not exposed again before the deposition and is not oxidized again. With these manufacturing steps, reliability of the semiconductor device is enhanced.

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L1: Entry 4 of 8 File: JPAB Sep 29, 1998

PUB-NO: JP410261635A
DOCUMENT-IDENTIFIER: JP 10261635 A
TITLE: SEMICONDUCTOR DEVICE

PUBN-DATE: September 29, 1998

INVENTOR-INFORMATION:
NAME COUNTRY
FUKADA, TETSUO
MORI, TAKESHI
HASEGAWA, MAKIKO
TOYODA, YOSHIHIKO

ASSIGNEE-INFORMATION:
NAME COUNTRY
MITSUBISHI ELECTRIC CORP

APPL-NO: JP09064108
APPL-DATE: March 18, 1997

INT-CL (IPC): H01 L 21/3205

ABSTRACT:

PROBLEM TO BE SOLVED: To suppress the release of a Cu wiring layer from surface by a method, wherein a trench is formed in an insulating layer to interpose an underneath layer in the trench for burying a Cu wiring layer to form a bonding layer covering the wiring layer further forming a cap layer covering the bonding layer.

SOLUTION: A trench 2 is formed in an insulating layer 1, made of silicon oxide film, etc., to form an underneath layer 3 made of TiN, etc., in the trench 2 further forming a Cu wiring layer 4 on the underneath layer 3. Next, a bonding layer 5 covering the Cu wiring layer 4 and the underneath layer 3 for increasing the bonding strength between a cap layer 6 and the Cu wiring layer 4 is formed. At this time, the bonding layer 5 is to be made of a material for the bonding strength between the bonding layer 5 and the Cu wiring layer 4 to exceed that between the Cu wiring 4 and the cap layer 6 as well as the growing rate of an oxide not exceeding that of the Cu wiring 4. Through these procedures, the connecting strength between the Cu wiring layer 4 and the cap layer 6 can be increased, also enabling the oxidation of the surface of the Cu wiring layer 4 to be suppressed effectively.

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L1: Entry 8 of 8 File: JPAB Jan 19, 1996

PUB-NO: JP408017920A
DOCUMENT-IDENTIFIER: JP 08017920 A
TITLE: SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

?

PUBN-DATE: January 19, 1996

INVENTOR-INFORMATION:

NAME	COUNTRY
IGUCHI, TOMOYUKI	

DB = Ti/TiN/Ti

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOSHIBA CORP	

APPL-NO: JP06148318
APPL-DATE: June 29, 1994

INT-CL (IPC): H01 L 21/768; H01 L 21/28

ABSTRACT:

PURPOSE: To provide a semiconductor device having a contact hole which is surely filled with electrode material metal and a buried wiring layer and a manufacturing method of the device.

CONSTITUTION: The semiconductor device consists of the following; a contact hole 14 formed in an SiO2 film 13 on a semiconductor substrate 11, a barrier metal film having a Ti film 21 and a TiN film 22 which are formed on the inner part of the contact hole and the whole surface of the SiO2 film 13, and a Ti film 23a formed on the TiN film 22 and the side wall part of the contact hole 14, and an Al alloy film 15 which is buried in the contact hole.